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- ☐ 1. Optimization of primitive gate networks using multiple output two-level m
Malik, A.A.;
Design Automation Conference, 1992. Proceedings., 29th ACM/IEEE
8-12 June 1992 Page(s):449 - 453
Digital Object Identifier 10.1109/DAC.1992.227761
[AbstractPlus](#) | Full Text: [PDF\(420 KB\)](#) IEEE CNF
- ☐ 2. Delay models for the sea-of-wires array synthesis system
Ing-Yi Chen; Geng-Lin Chen; Sy-Yen Kuo;
European Design and Test Conference, 1995. ED&TC 1995, Proceedings.
6-9 March 1995 Page(s):228 - 232
Digital Object Identifier 10.1109/EDTC.1995.470398
[AbstractPlus](#) | Full Text: [PDF\(368 KB\)](#) IEEE CNF
- ☐ 3. A novel genetic algorithm for the automated design of performance drive
Hounsell, B.I.; Arslan, T.;
Evolutionary Computation, 2000. Proceedings of the 2000 Congress on
Volume 1, 16-19 July 2000 Page(s):601 - 608 vol.1
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Partitioned ROBDDs—a compact, canonical and efficiently...

Probabilistic verification of Boolean functions, Formal Methods in System Design, ...
 1, 1992, 17. Jawahar Jain, Rajesh Mukherjee, Masahito Fujita, ...
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ps) published in Proceedings of the International Workshop on Logic ...
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 Design, volume 1, pages 63-117, 1992. [M86] Jean-Christophe Madre and ...
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- ☐ 1. Fast algorithm for computing spectral transforms of Boolean and multiple functions on circuit representation
Krenz, R.; Dubrova, E.; Kuehnemann, A.;
Multiple-Valued Logic, 2003. Proceedings. 33rd International Symposium on
16-19 May 2003 Page(s):334 - 339
Digital Object Identifier 10.1109/ISMVL.2003.1201426
AbstractPlus | Full Text: PDF(439 KB) IEEE CNF

- ☐ 2. Improved fault detection using a selected grouping of parity equations for flight control systems
Sudano, J.J.; Preisig, J.R.; Pokchylo, J.;
Aerospace and Electronics Conference, 1988. NAECON 1988., Proceedings of
National
23-27 May 1988 Page(s):1565 - 1569 vol.4
Digital Object Identifier 10.1109/NAECON.1988.195218
AbstractPlus | Full Text: PDF(372 KB) IEEE CNF

- ☐ 3. Optimization of multiple-valued AND-EXOR expressions using multiple-p diagrams
Sesao, T.;
Multiple-Valued Logic, 1992. Proceedings., Twenty-Second International Symp
27-29 May 1992 Page(s):451 - 458
Digital Object Identifier 10.1109/ISMVL.1992.186830
AbstractPlus | Full Text: PDF(624 KB) IEEE CNF

- ☐ 4. A functionality fault model: feasibility and applications
Zemva, A.; Biglez, F.; Kozminski, K.; Zolc, B.;
European Design and Test Conference, 1994. EDAC, The European Conferen
Automation. ETC European Test Conference. EUROASIC, The European Eve
Design. Proceedings.
28 Feb.-3 March 1994 Page(s):152 - 158
Digital Object Identifier 10.1109/EDTC.1994.326883
AbstractPlus | Full Text: PDF(696 KB) IEEE CNF

- ☐ 5. CARLOS: an automated multilevel logic design system for CMOS semi-circuits
Mathony, H.-J.; Ballinger, U.G.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transaction

Volume 7, Issue 3, March 1988 Page(s):346 - 355
Digital Object Identifier 10.1109/43.3168
AbstractPlus | Full Text: PDF(728 KB) IEEE JNL

- ☐ 6. Improving area efficiency of residue number system based implementation algorithms
Mahesh, M.N.; Gupta, S.; Mehendale, M.;
VLSI Design, 1999. Proceedings. Twelfth International Conference On
7-10 Jan. 1999 Page(s):340 - 345
Digital Object Identifier 10.1109/CVD.1999.745179
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 **PALM INTRANET**Day : Tuesday
Date: 8/2/2005
Time: 21:16:38**Inventor Name Search Result**

Your Search was:

Last Name = HOARE

First Name = RAYMOND

Application#	Patent#	Status	Date Filed	Title	Inventor Name
<u>60673715</u>	Not Issued	020	04/21/2005	METHOD AND DEVICE FOR REDUCING POWER CONSUMPTION OF ACTIVE RFID TAGS	HOARE, RAYMOND R.
<u>60672347</u>	Not Issued	020	04/18/2005	METHOD FOR AUTOMATIC GENERATION OF SOFTWARE FOR INTEGRATED CIRCUIT MICROPROCESSORS	HOARE, RAYMOND R.
<u>60571250</u>	Not Issued	159	05/13/2004	HARDWARE ACCELERATED SPEECH RECOGNITION	HOARE, RAYMOND
<u>60267529</u>	Not Issued	159	02/09/2001	DISCRETE EVENT LOGIC SIMULATION ENGINE	HOARE, RAYMOND R.
<u>10043847</u>	Not Issued	030	01/11/2002	DISCRETE EVENT SIMULATOR	HOARE, RAYMOND R.

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Your Search was:

Last Name = AHN

First Name = JIYONG

Application#	Patent#	Status	Date Filed	Title	Inventor Name
10100027	Not Issued	061	03/19/2002	APPARATUS FOR STRIPPING FIBRIN FROM A CATHETER	AHN, JIYONG
10043847	Not Issued	030	01/11/2002	DISCRETE EVENT SIMULATOR	AHN, JIYONG

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Your Search was:

Last Name = GRAVES

First Name = JESSE

Application#	Patent#	Status	Date Filed	Title	Inventor Name
<u>29197013</u>	Not Issued	071	01/08/2004	ROSE SCULPTURE	GRAVES, JESSE
<u>10043847</u>	Not Issued	030	01/11/2002	DISCRETE EVENT SIMULATOR	GRAVES, JESSE

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